MECL III

ADVANCE INFORMATION SECTION

INTRODUCTION

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry, in general, has recognized that the only economical way to obtain high system operating speed is through the use of emitter-coupled logic. As the result of considerable effort in research and development, Motorola offers a state-of-the-art, emitter-coupled logic family with sub-nanosecond local propagation delays – MECL III.

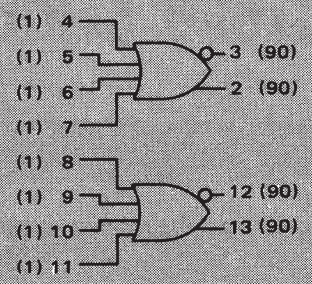
MECL III circuit design is similar to that employed in the popular MECL II family. In the MECL III line, however, more advanced processing techniques are employed and the capability of driving low-impedance terminated lines is provided.

INITIAL MECL III INTRODUCTIONS

LOGIC DIAGRAMS (V_{CC} = GND = PINS 1 AND 14: V_{EE} = -5.2 V ± 10% = STUD)

Loading Factors Listed Below Are dc Unterminated.

MC1660S
Dual 4-Input OR/NOR Gate

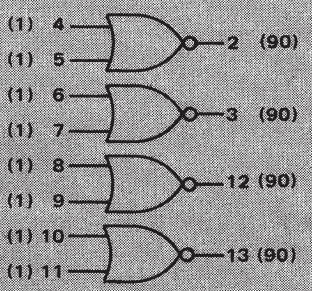


$3 = \overline{4+5+6+7}$

$2 = 4+5+6+7$

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 110 mW typ/pkg (no load)

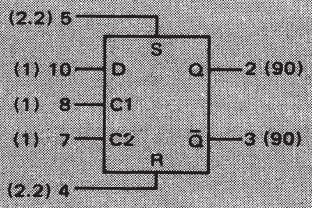
MC1662S
Quad 2-Input NOR Gate



$2 = \overline{4+5}$

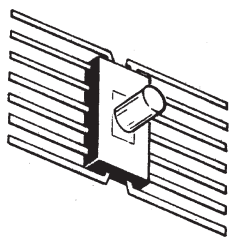
t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (no load)

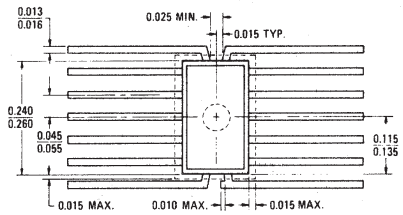
MC1670S
Single Phase Type D Flip-Flop

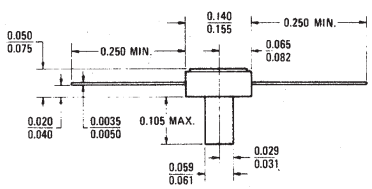


f_{Tog} = 350 MHz typ
P_D = 190 mW typ/pkg (no load)

MECL III STUD PACKAGE







NOTE: Lead No. 1 is identified by a tab on that lead.

CASE 617
OUTLINE DIMENSIONS

MECL III DESIGN PHILOSOPHY

The following goals have been met by MECL III, resulting in the highest performance logic family obtainable.

1. Gate switching speeds of 1 ns
2. Capability of driving terminated lines with impedance as low as 50 ohms
3. Flip-flop toggle and shifting rate greater than 300 MHz
4. Operation with unused inputs left open
5. Multilayer metalization for optimum performance
6. New packages with improved electrical and thermal characteristics
7. Compatability with low-cost MECL II

MECL III has satisfactorily met its design goals. Speeds are in the subnanosecond region with local fan-out loading, and are slightly above 1 ns driving a 50-ohm load.

Family Characteristics

0.9 ns propagation delay time into 510-ohm load

1.1 ns delay time into 50-ohm load

Fan-out of 5 "low-impedance" inputs

Fan-out of multiple "high-impedance" inputs with 50-ohm terminations to −2.0 V

Power dissipation of 55 mW per logic gate

Binary speeds of 350 MHz

Packaging

The standard MECL III package is a stud-mounted, 15-pin ceramic flat pack. The stud, which is connected to V_{EE}, is designed to significantly improve heat dissipation. It is designated pin 15 in schematic representation of the circuits.

Advantages of MECL III Circuits

High-speed operation – relatively unaffected by temperature and supply voltage variations

50-ohm driving capability

Minimal system crosstalk and noise generation

Compatibility with MECL II

V_{BB} and logic swing compensated for voltage and temperature variations

Single power supply operation

Implied OR (Wired OR) capability

Complementary outputs

Multi-level gating

Expansion into high-speed MSI-LSI

GENERAL CHARACTERISTICS OF MECL III INTEGRATED CIRCUITS

The MECL III logic family is designed for very high speed digital system operation. Gate circuits are capable of subnanosecond speeds with local fan-out loading and of driving terminated lines with 1.5-ns rise times and 1.1-ns propagation delays.

Basic Gate

The basic MECL III gate, a 4-input OR/NOR, is shown in Figure 1. In reviewing the operation of this circuit, assume that the inputs to transistors 1 thru 4 initially are either open or tied to a logical "0" level. With these input conditions, Q1 thru Q4 will be "off" and Q5 will be turned "on" with a current flow controlled by the internal bias-voltage regulator and the value of R_E. The emitter of Q7 (with a load) will be at a logical "1" and the emitter of Q8 will be at logical "0". Now let the voltage on the base of

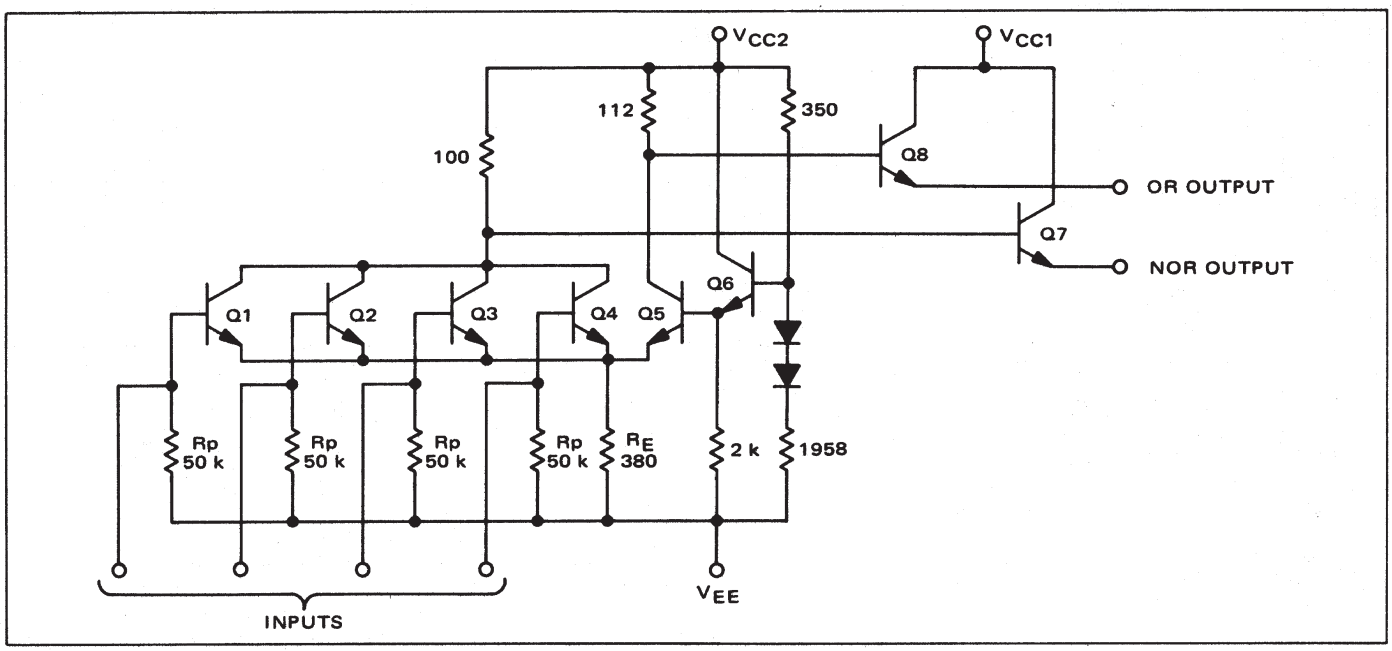


FIGURE 1 – BASIC HIGH INPUT IMPEDANCE MECL III GATE

Q1 be brought toward ground; when it approaches −1.300 V (the bias voltage applied to the base of Q5), transistor Q1 will start conducting and the current through Q5 will start to decrease. When the Q1 base voltage reaches a logical "1" level (−0.800 V nominal into a 510-ohm load), transistor Q5 will be "off" and Q1 will conduct. The voltage at the common-emitter node will be one base-emitter drop below the base of Q1 or at a logical "0" level (−1.70 V). If the Q1 base voltage is allowed to continue toward ground, Q1 will start to saturate at an input of approximately −0.40 V. The transfer characteristics of the basic gate are shown for a variety of temperatures in Figure 2. A more complete description of the basic MECL gate operation is given in the general information section of the MECL II brochure. MECL III circuit operation is similar, although voltage and current levels are somewhat different.

Noise Considerations

In designing the MECL III circuits for minimum propagation delay, it is necessary to employ a separate V_{CC} line for supplying current to the output devices. This separation of V_{CC} lines prevents current transients, due to unbalanced loading of the output devices, being coupled back into the gate by way of common connections to a V_{CC} node. For the best results in characterization and in system performance, these terminals should be connected to a good ground plane close to the package. The connection for the bias driver and input circuit is designated V_{CC2}, and is connected via pin 14. The output device supply is labeled V_{CC1} and is connected to pin 1.

Input Pulldown Resistors

There is an input pulldown resistor (Rp) associated with each input in the MECL III family. This resistor circumvents the "floating base" problem in emitter-coupled logic families by providing a sink for I_{CBO} leakage currents and for signals that would normally be coupled to a floating base through C_{ob}. Pulldown resistor value for the high-input impedance circuits is ≧ 50-kilohms.

A soon-to-be announced group of circuits will employ 2-kilohm pulldown resistors. In these circuits, the resistor will not only serve as a pulldown for floating bases, but will act as a load for the output device of the driving gate. Figure 3 shows the effect of loading a gate that has no output load resistor with a fan-out of gates having low-input impedance load resistors (2-kilohm). Note that the curve is relatively flat. A well designed printed circuit board with tight inter-package spacing (0.625 in. between centers) would be a candidate for such loading techniques.

Output Loading and Transmission Line Driving

The MECL III emitter follower output devices are designed to drive a 50-ohm transmission line terminated to −2.0 V. This is an equivalent output load current of 22 mA. When terminated with a 510-ohm resistor to V_{EE}, the emitter follower output current is 8.5 mA. The effects of temperature and power supply variation on propagation delay time for these terminations can be seen in Figures 4 and 5.

Figure 6 shows the variation in t_{pd}, due to capacitive loading. To avoid the feedback effects of loop testing

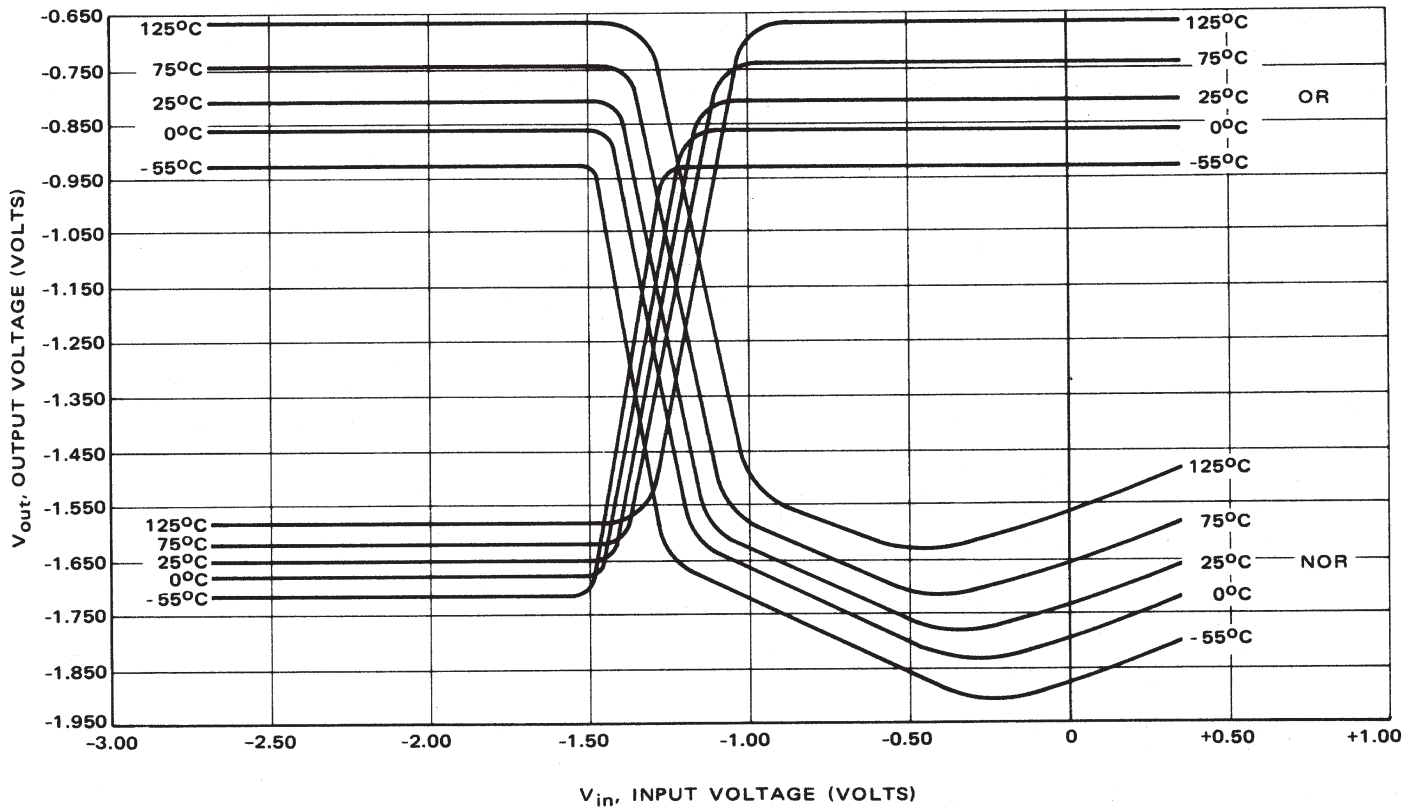


FIGURE 2 – MC1660S (510-OHM LOAD) TRANSFER CHARACTERISTICS

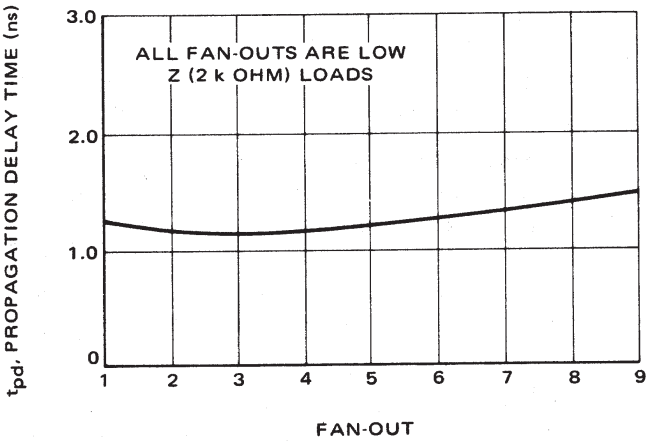


FIGURE 3 – AVERAGE PROPAGATION DELAY TIME versus FAN-OUT

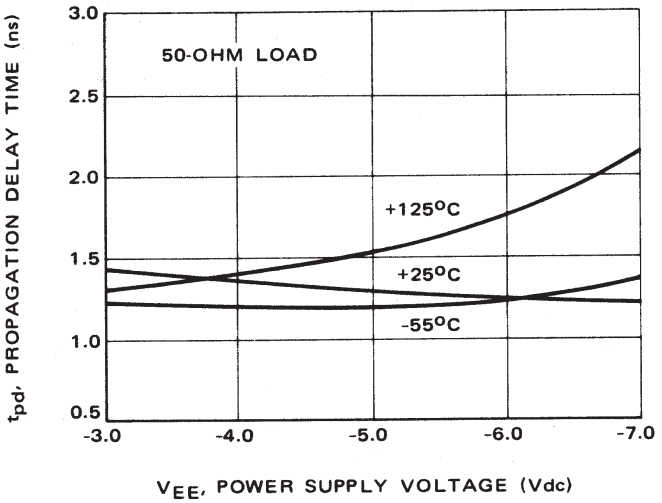


FIGURE 4 – AVERAGE PROPAGATION DELAY TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

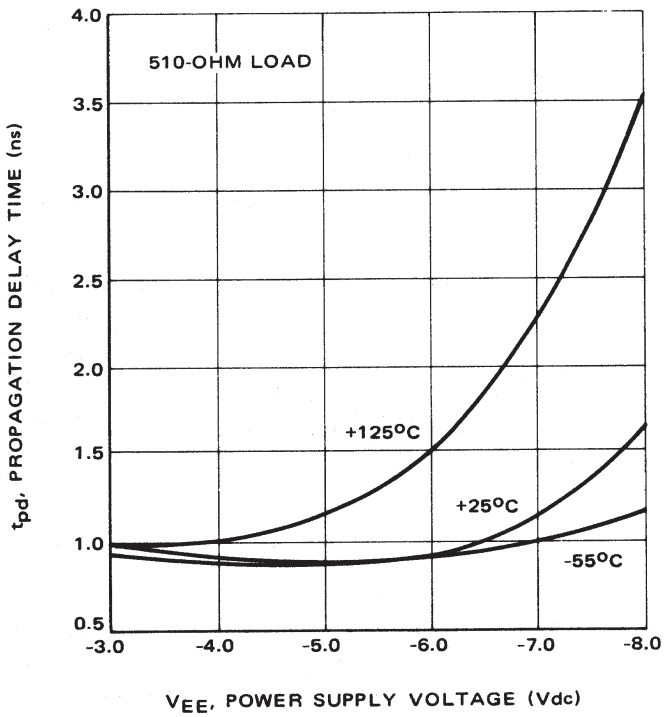


FIGURE 5 – AVERAGE PROPAGATION DELAY TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

(described under characterization and shown in Figure 9) a generator was used to drive the circuit under test.

The connection for driving a parallel terminated transmission line is shown in Figure 7. With a full logic swing available at both ends of the line, it is possible to drive fan-out at either end and also at various points along the transmission line.

A currently popular approach is the series-terminated transmission line (see Figure 8). This differs from parallel termination in that a one-half logic swing is propagated through the transmission line. This logic swing doubles at the end of the transmission line due to the reflection of an

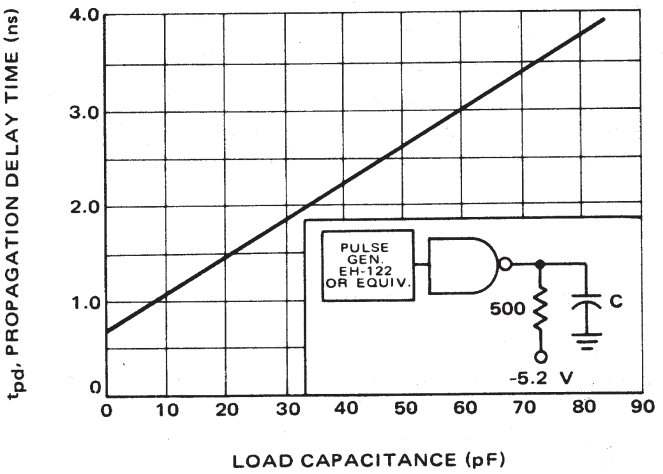


FIGURE 6 – AVERAGE PROPAGATION DELAY TIME versus LOAD CAPACITANCE

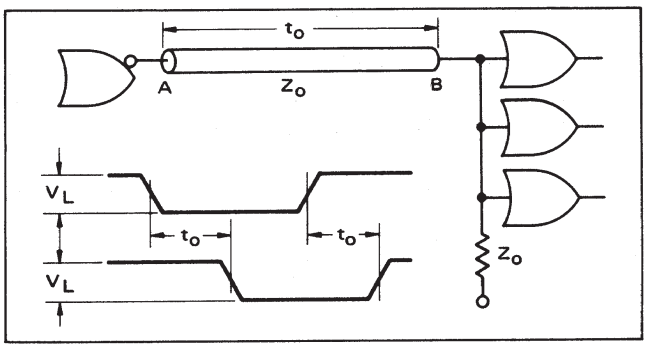


FIGURE 7 – DRIVING A PARALLEL TERMINATED LINE

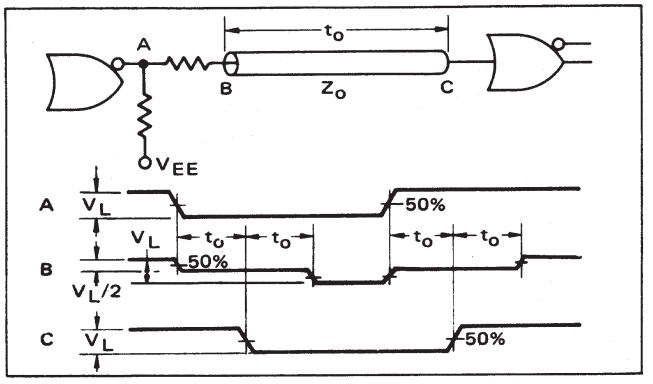


FIGURE 8 – DRIVING A SERIES TERMINATED LINE

open line, thus establishing a full logic swing again. To keep clean wave fronts, it is required that the input impedance of the driven gate be much greater than the characteristic impedance of the transmission line. That condition is satisfied by the design of MECL III. Using the appropriate pulldown at point A, the reflections in the transmission line are terminated. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing and reflections.

Characterization Techniques for High-Speed MECL III Circuits

DC – The transistors used in the MECL III circuit designs have f_T values of approximately 2 GHz. For this reason, even though the gates have positive input impedances, care must be taken in the assembly of dc test fixtures to avoid feedback paths which might cause oscillation. Good quality high-frequency capacitors should be used to decouple the power supplies. In addition, capacitors may be needed across the outputs where excessively long lead lengths are used and a large amount of coupling may be experienced. Also helpful is the use of ferrite oscillation-suppression beads on all input and output wires.

AC – When making ac measurements on MECL III circuits, the power supplies should be decoupled with high frequency capacitors. This is particularly necessary when a socket is being used to test the gate. In addition, when coaxial cable is used, the shield should be soldered to a good ground plane within 1/8 to 3/16 inch of the cable center conductor.

Motorola uses the test setup shown in Figure 9 to avoid the problems associated with variations in the rise times of pulse generators. Note that the circuit drives itself through a specified length of coaxial cable. Using this technique, the results obtained on a specific test fixture should be unchanging over any period of time, and should be dependent only upon the repeatability of the oscilloscope calibration and accuracy.

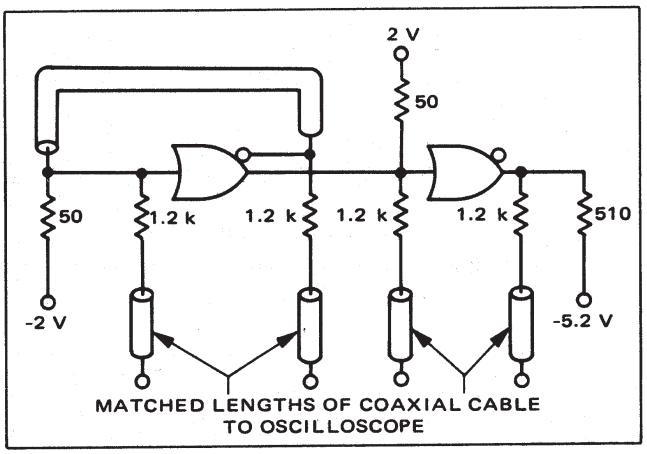


FIGURE 9 – AC TEST FIXTURE

Gate Characteristics

V_{OL}	Logical "0" Level	–1.700 V
V_{OH}	Logical "1" Level	–0.800 V
NM "0"	Logical "0" Noise Margin	0.240 V
NM "1"	Logical "1" Noise Margin	0.240 V
FO	DC Fanout	90
P_D	Power Dissipation (per gate)	55 mW
t_{pd}	Propagation Delay (50-ohm load)	1.1 ns
	Propagation Delay (510-ohm load)	0.9 ns

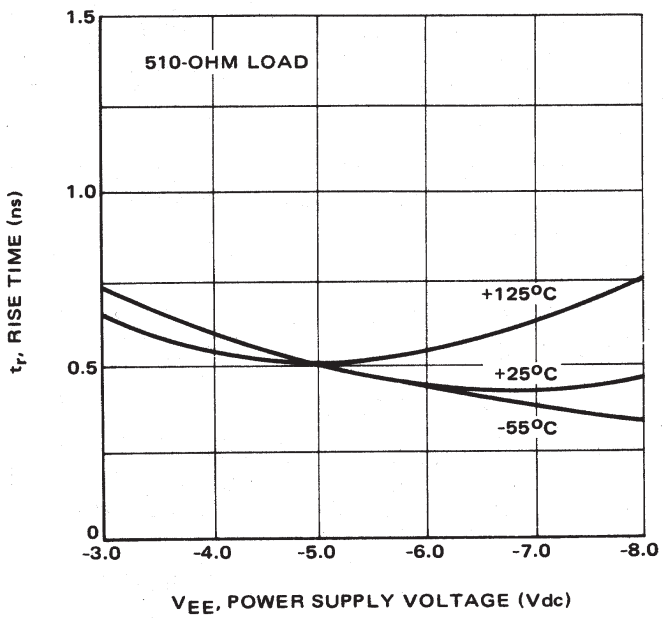


FIGURE 10 – RISE TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

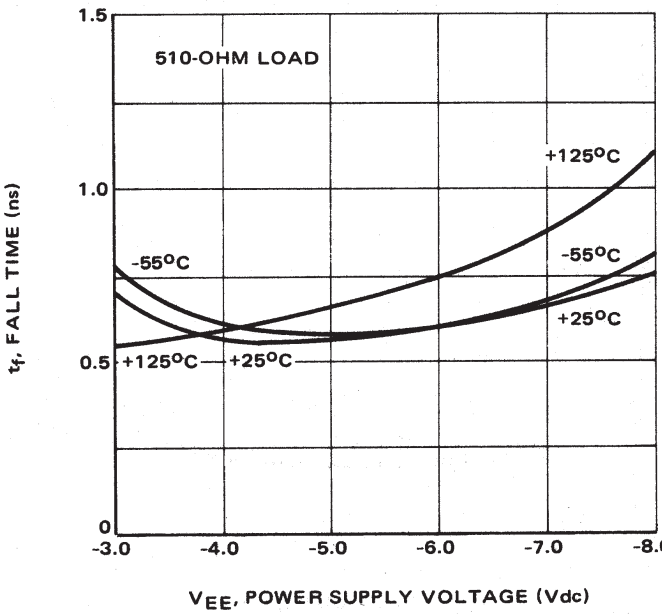


FIGURE 11 – FALL TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

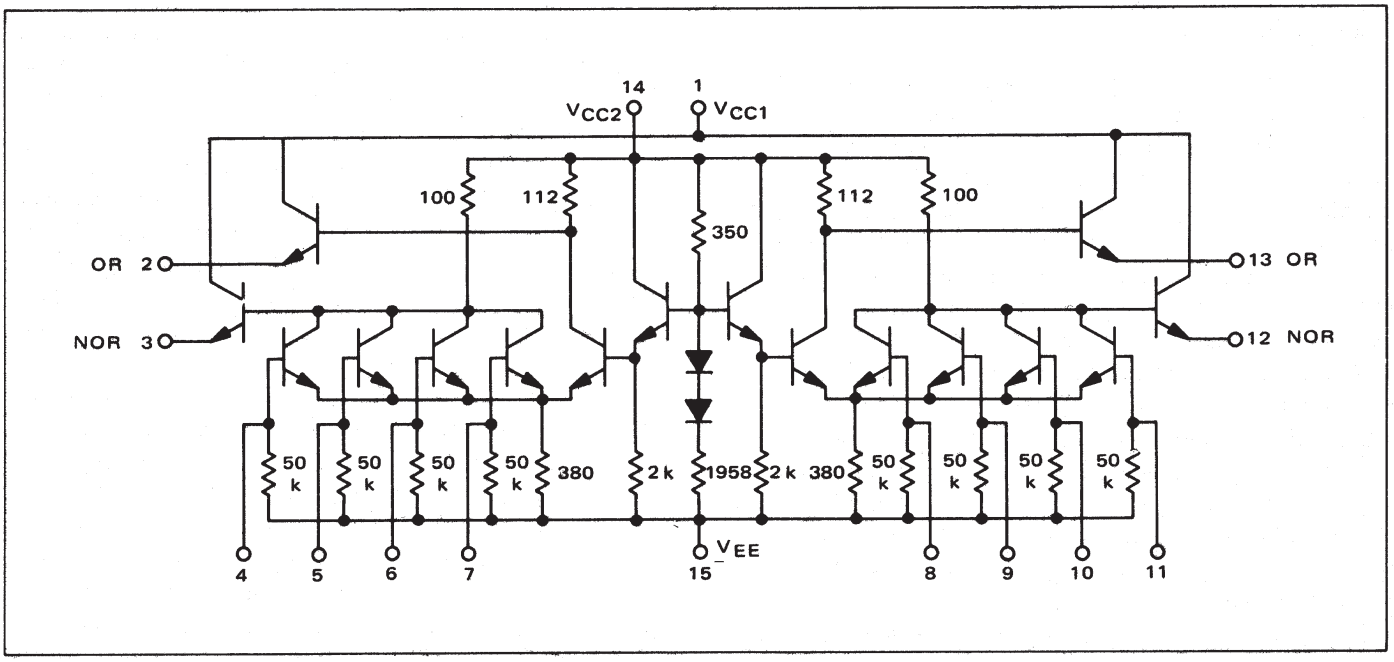


FIGURE 12 – DUAL 4-INPUT OR/NOR GATE (MC1660S)

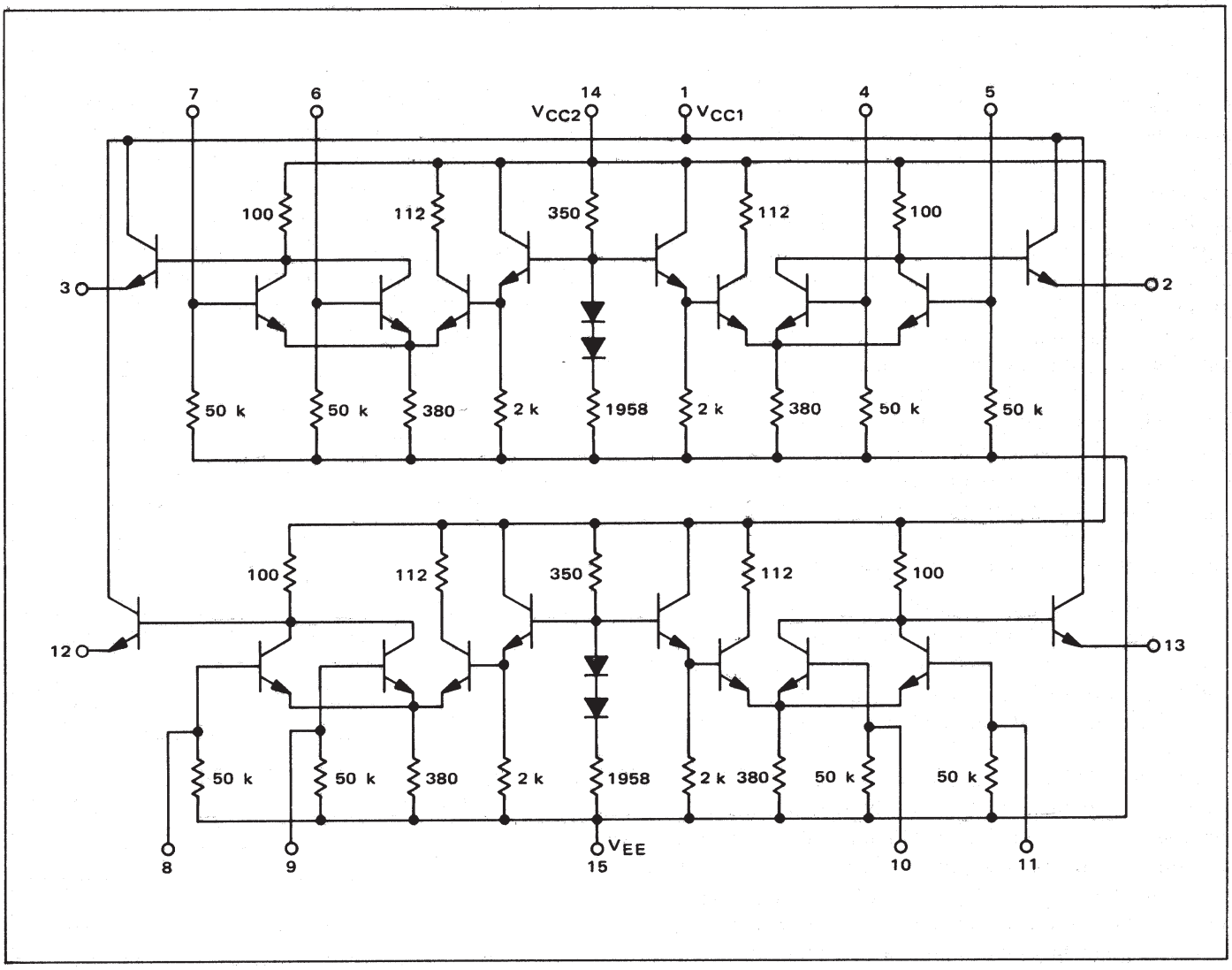


FIGURE 13 – QUAD 2-INPUT NOR GATE (MC1662S)

Flip-Flop Characteristics

To complement the gate elements of the MECL III family, a storage element capable of shifting and counting with very low propagation delay time is required. An all-logic type D flip-flop has been selected for the initial introduction. This circuit, the MC1670S, has been designed using two layers of metal to provide a more economical, reduced chip size device. It not only offers high speed, but simplifies system application since operation is not dependent on clock rise time.

A more exact title for this flip-flop is "one-phase D". (It is similar to the MECL II MC1022 and MC1034.) The MC1670S is a master-slave flip-flop with an information or data input to the master. The master is updated while the clock is at a low level, and data is transferred to the slave on a positive excursion of the clock. Direct set and reset inputs are provided for pre-setting or parallel data entry. These set and reset inputs are provided with a "look ahead" capability since both the master and slave sections are changed simultaneously by the direct inputs. Figures 14 and 15 illustrate logical operation of the single phase type D flip-flop.

Operation of the Single Phase Type D Flip-Flop

In the circuit of Figure 16 assume that initially Q, C, R, S, and D are at "0" levels and that $\overline{Q}$ is at the "1" level. Since the clock is low, transistors 1Q3 and 2Q3 are conducting. In the slave section, only transistors 2Q6 and and 2Q7 are in series with 2Q3. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through 1Q3 and 1Q9.

Now assume that the data input goes high. The high-input signal on the base of 1Q4 causes it to conduct, and 1Q9 to turn "off". The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of 1Q11. Since there is essentially no current flow through RC2, the base of transistor 1Q10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of 1Q6. 1Q6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor 1Q2 turns "on" and transistor 1Q3 turns "off". This provides a current path for the common-emitter transistors 1Q5, 1Q6, 1Q7, and 1Q8. Since the bases of all these devices except 1Q6 are in the low state, current flow is through 1Q6. This maintains the base and emitter of 1Q11 low, and the base and emitter of 1Q10 high. The high state on 1Q10 is transferred to 2Q4 of the slave section. As the clock continues to rise 2Q2 begins to turn "on" and 2Q3 to turn "off". (Reference voltages in the master and slave units are slightly offset to insure prior clocking of the master section.) With transistor 2Q2 conducting and the base of 2Q4 in a high state, the current path now includes 2Q2, 2Q4, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of 2Q11. The lack of current flow through RC4 causes a high state input to the base of 2Q10. These states are once again fed back to the latch transistors, 2Q6 and 2Q7.

As the clock voltage falls, transistor 2Q2 turns "off" and 2Q3 turns "on". This provides a current path through the latch transistors, "locking in" the slave output.

In the master section the falling clock voltage turns "on" transistor 1Q3 and turns "off" 1Q2. This enables the input transistor 1Q4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs 1Q2:1Q3 and 2Q2:2Q3. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors 2Q4 and 2Q9. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the $\overline{Q}$ output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logical "1" level is applied to the S input transistor, 1Q2 begins to conduct because its base is now being driven through 1Q18 which is in turn connected to S. Transistor 1Q5 is now "on" and the feedback devices 1Q6 and 1Q7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors 2Q2, 2Q5, 2Q6, and 2Q7.

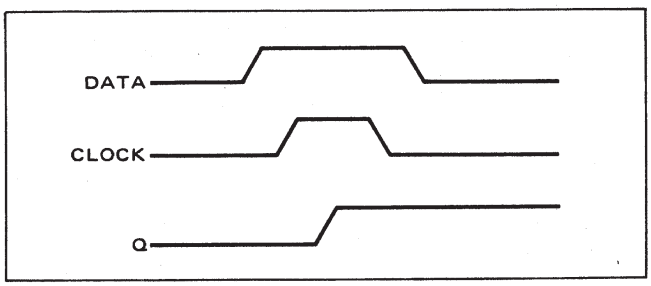


FIGURE 14 – SINGLE PHASE TYPE D OPERATION

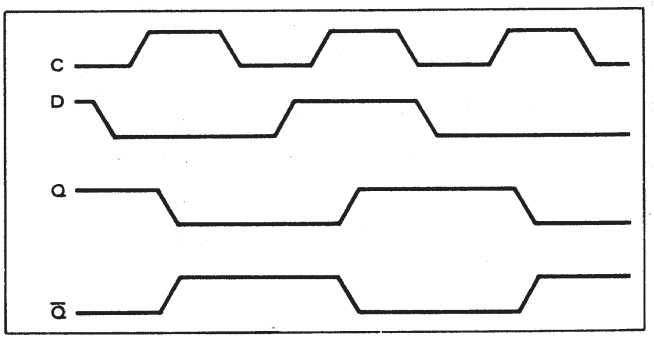


FIGURE 15 – SINGLE PHASE TYPE D FLIP-FLOP TIMING DIAGRAM

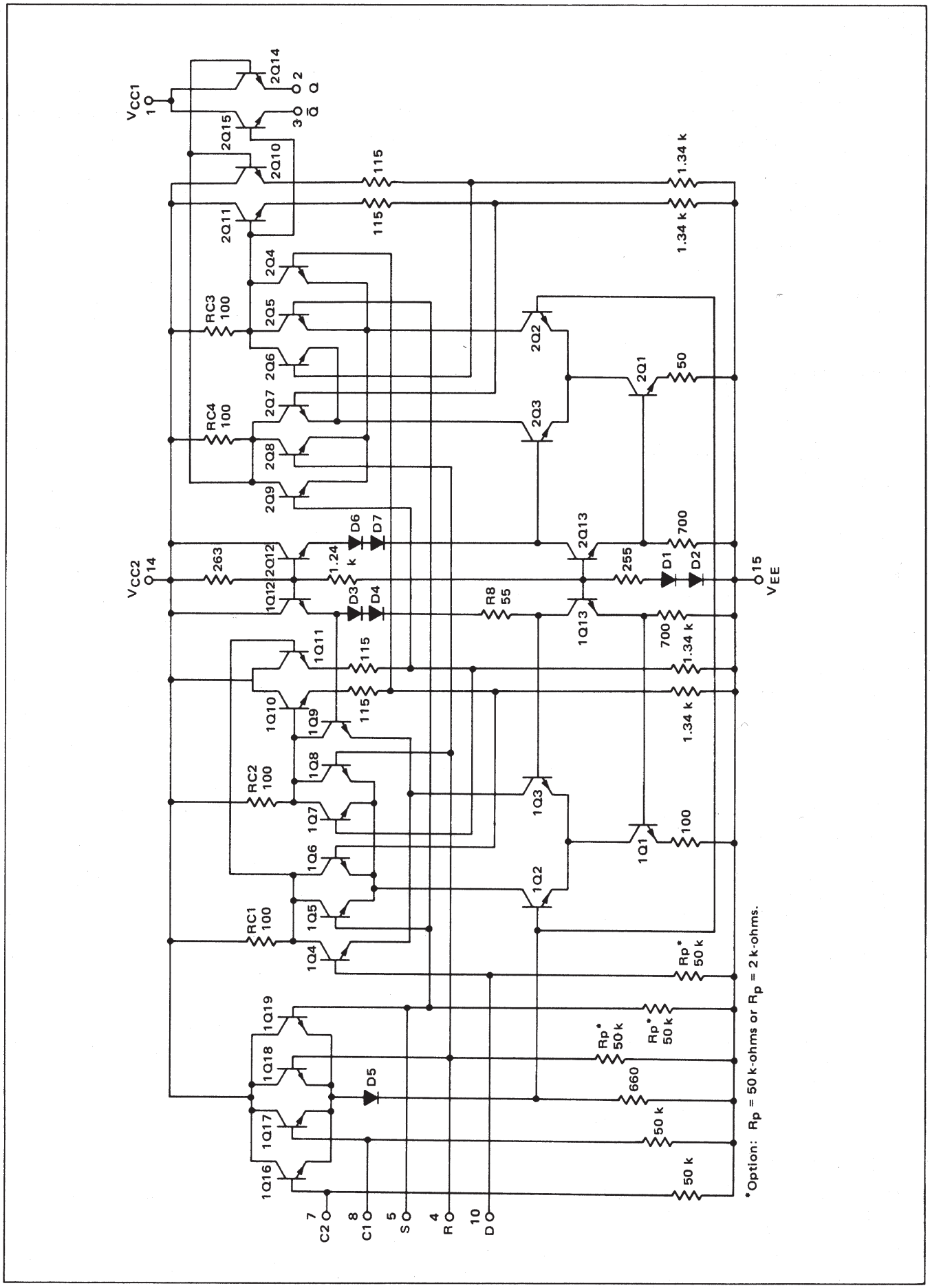


FIGURE 16 – MECL III SINGLE PHASE TYPE D FLIP-FLOP (MC1670S)

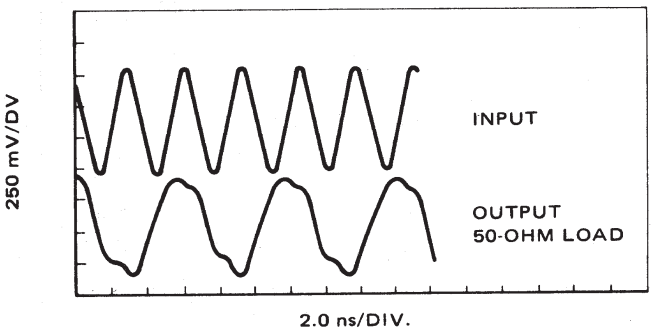


FIGURE 17 – MECL III SINGLE PHASE TYPE D FLIP-FLOP, 300 MHz TOGGLE OPERATION

Toggle Frequency

Minimum toggle frequency of the MC1670S is 300 MH: The waveform at 300 MHz is shown in Figure 17. By shif ing the bias voltage of the input waveform slightly, ove driving the clock input (≈ 1.0 volt), and shifting the powe supply approximately 10 percent more negative, it is po sible to "tweak" many of these flip-flops to 500 MHz. (Se Figure 18.) However, normal operation at this frequenc is not guaranteed and it is advisable to operate at 400 MH or less. A typical plot of maximum frequency versus ten perature is shown in Figure 19.

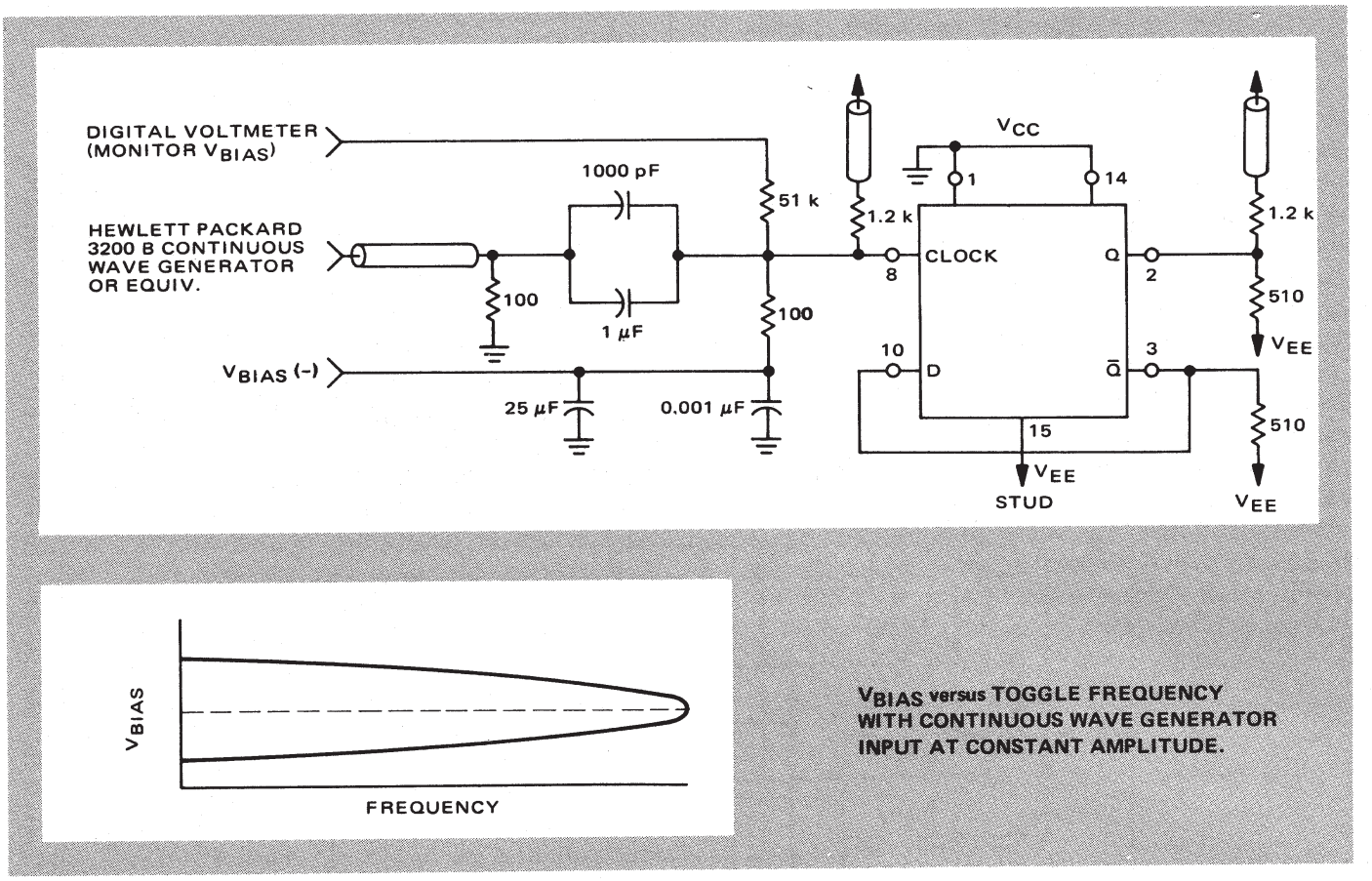


FIGURE 18 – SINGLE PHASE TYPE D MAXIMUM FREQUENCY TESTER

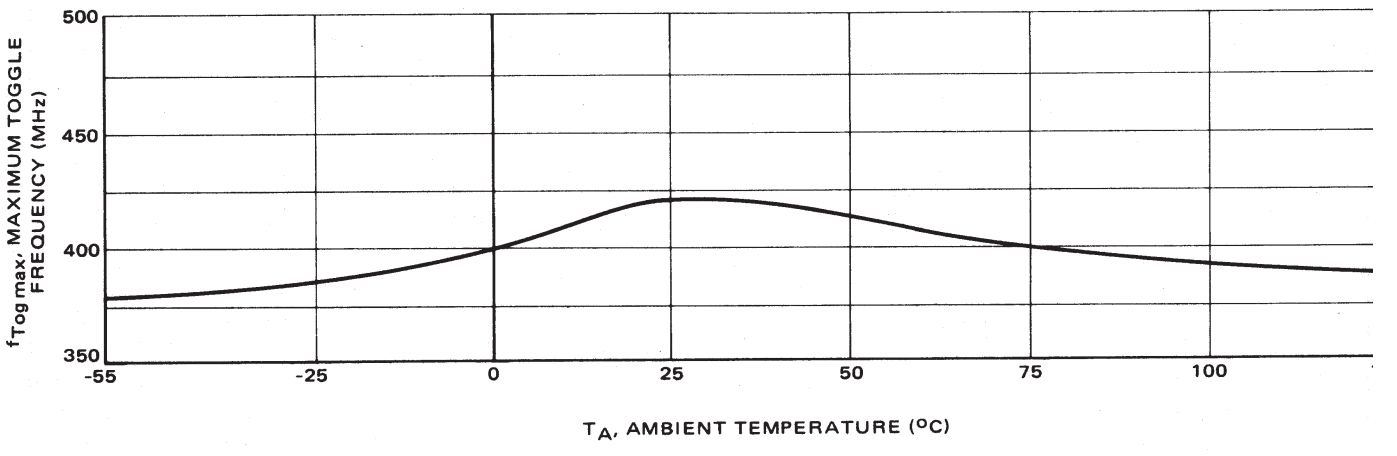


FIGURE 19 – MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE

Minimum Clock Up-and-Down Times

With the narrowest pulse width attainable using the normal rise and fall times experienced with MECL III and 510-ohm loading, it can be seen from Figures 20 and 21 that the flip-flop is still operating; this indicates that no problems with minimum clock widths are normally encountered. This will be true provided that a nominal logic swing is always available at the clock input.

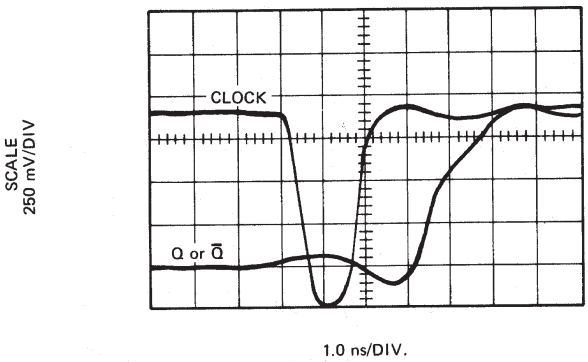


FIGURE 20 – MINIMUM "DOWN TIME" TO CLOCK LOADING = 510 Ω

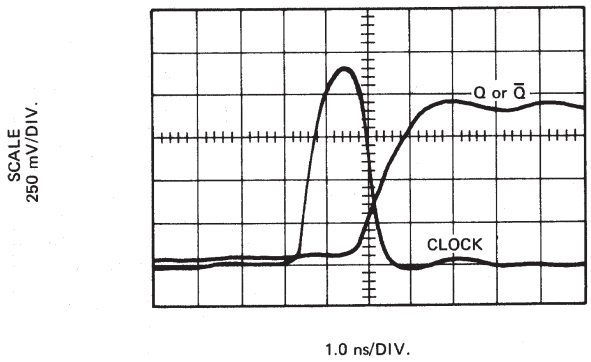


FIGURE 21 – MINIMUM "UP TIME" TO CLOCK LOADING = 510 Ω

Planned Additions

The initial introductions of the MECL III line are only the first of a broad line to come. Among the first of the additional parts will be gates with low impedance (2-kilohm input pulldown resistors). In addition there will be both low and high impedance OR gates to complement the quad 2-input NOR gates.

In the sequential circuit area, the next introductions will be a dual clocked R-S flip-flop and a dual type D latch. The primary advantage of these flip-flops lies in the availability of two high-speed functions per package.

Also planned for early introduction is an 8-bit full adder, MC1684F. In addition to being an extremely useful device, the full adder is the vanguard of MECL III complex functions.

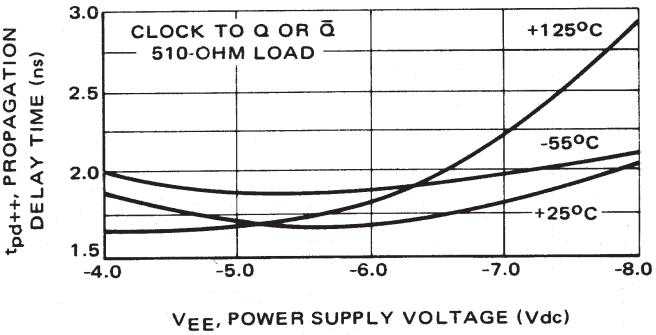


FIGURE 22 – AVERAGE PROPAGATION DELAY versus TEMPERATURE AND POWER SUPPLY

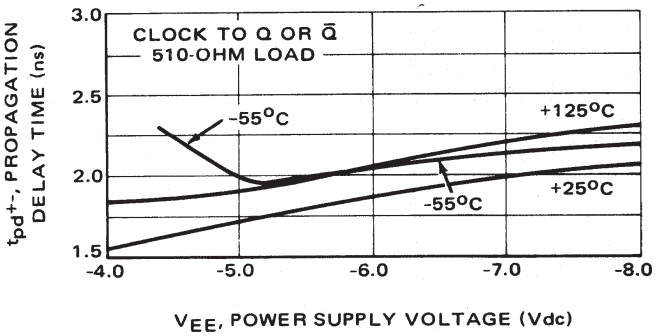


FIGURE 23 – AVERAGE PROPAGATION DELAY versus TEMPERATURE AND POWER SUPPLY

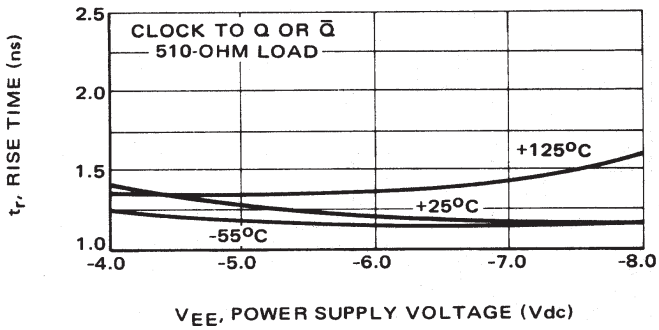


FIGURE 24 – RISE TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

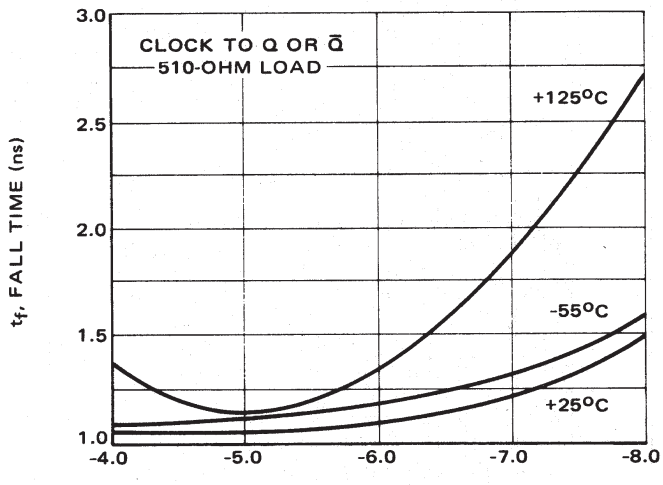


FIGURE 25 – FALL TIME versus TEMPERATURE AND POWER SUPPLY VOLTAGE

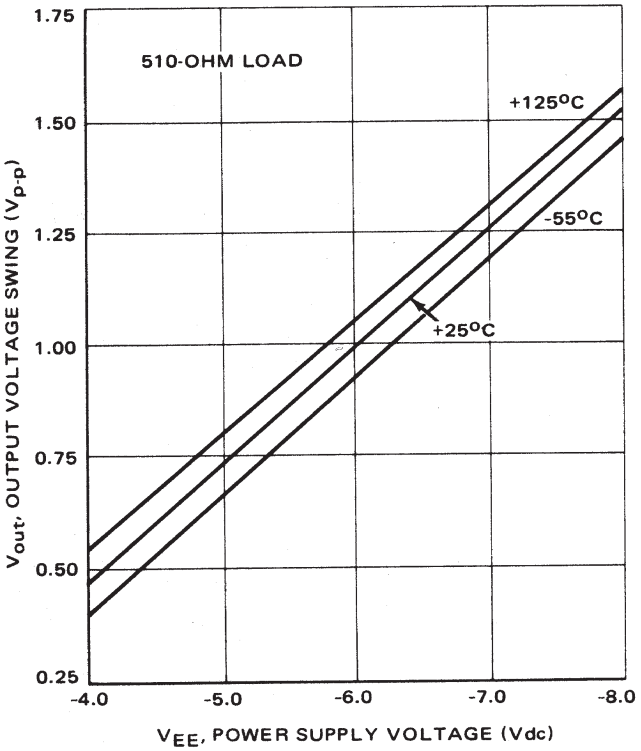


FIGURE 26 – OUTPUT VOLTAGE SWING versus TEMPERATURE AND POWER SUPPLY VOLTAGE

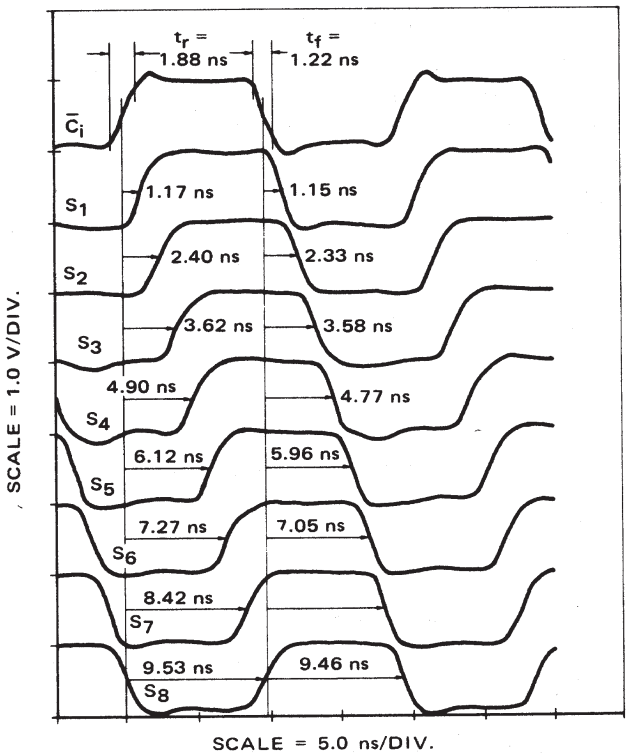
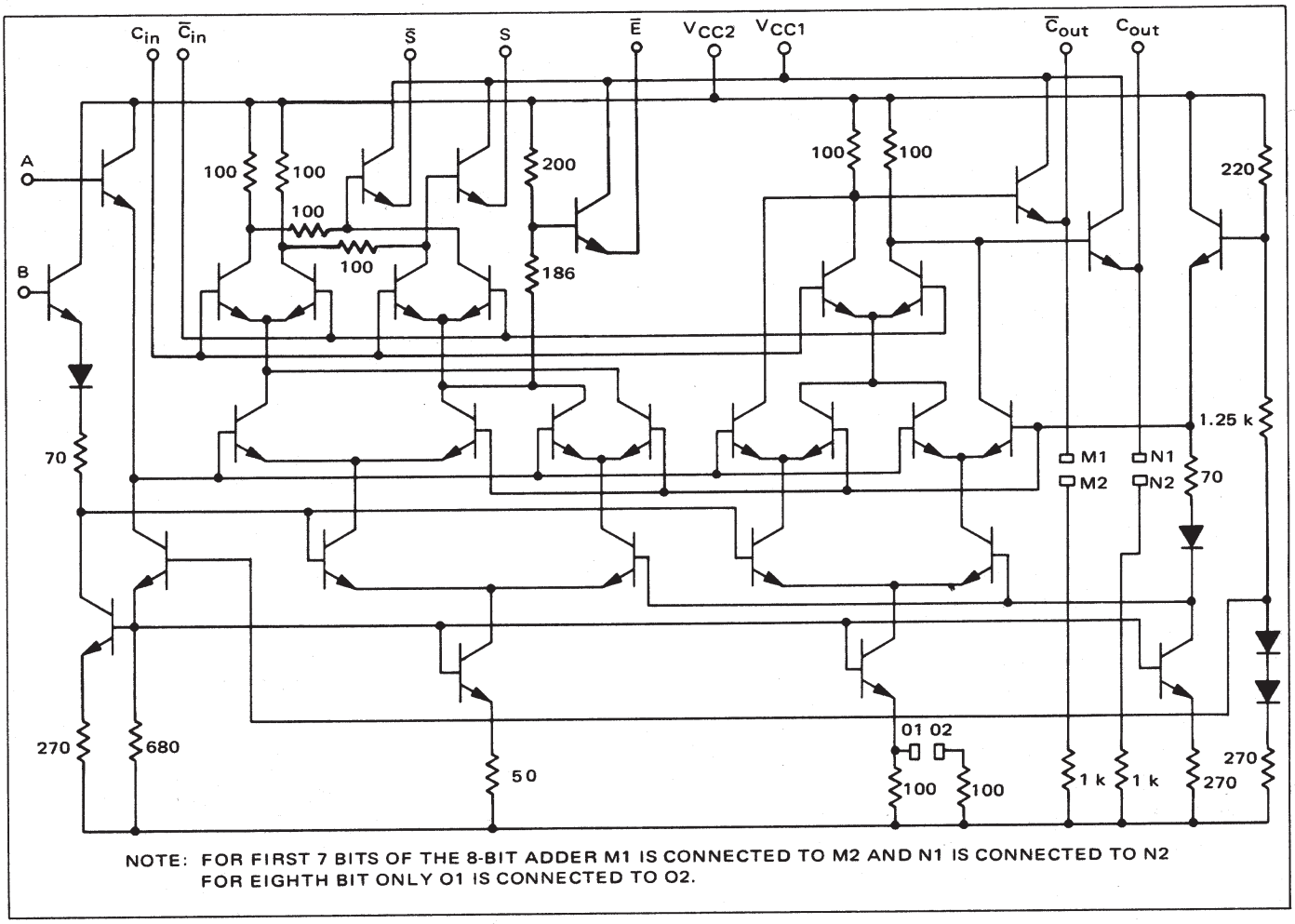


FIGURE 27 – CARRY-IN COMPLEMENT, $\bar{C}_i$, TO SUM OUT, S, DELAY OF MECL 8 BIT-ADDER



NOTE: FOR FIRST 7 BITS OF THE 8-BIT ADDER M1 IS CONNECTED TO M2 AND N1 IS CONNECTED TO N2
FOR EIGHTH BIT ONLY O1 IS CONNECTED TO O2.

FIGURE 28 – 1-BIT SINGLE FULL ADDER

This 8-bit adder is equivalent to 88 logic gates and is fabricated with three layers of metalization. The device employs a total of 448 components. The die size enclosed by the perimeter along the outer edge of the bonding pads is 46.3 x 110.1 mils with a resulting area of 5098 square mils. The effective average component area, therefore, is 11.4 square mils per component. With all of its complexity, the adder offers true MECL III speed. The per-stage delay from CARRY-IN to SUM-OUT is approximately 1.2 ns. Connected as an 8-bit ripple-carry adder, total delay from CARRY-IN to SUM-OUT of the 8-bit is only approximately 10 ns (see Figure 27).

The 8-bit adder is composed of four subgroups, each consisting of dual full adders. The basic MECL III full adder is a subgroup of 56 components interconnected with series gating techniques to produce the full adder function with a minimum propagation delay. Figure 28 shows the series gating structure for a single full adder. Figure 29 illustrates the logic performed by a single full adder and Figure 30 shows the interconnection of the 8-individual full adder functions. Both the SUM and $\overline{SUM}$ are available for each bit and are made available at the outputs. The $\overline{E}$ function, internally wire OR-ed, is also brought out.

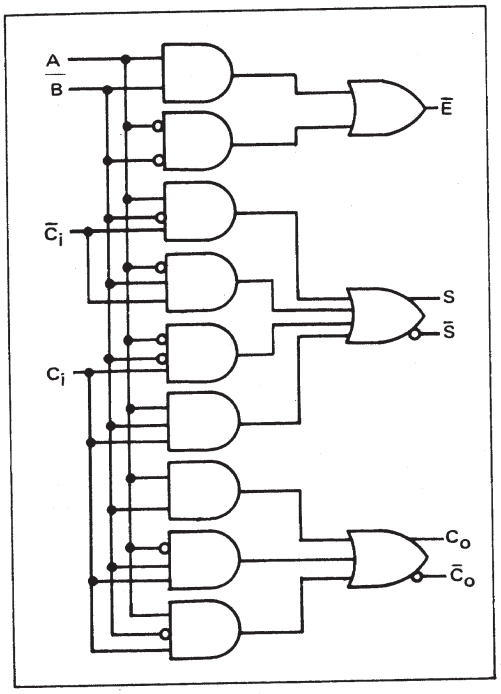


FIGURE 29 – 1-BIT SINGLE FULL ADDER

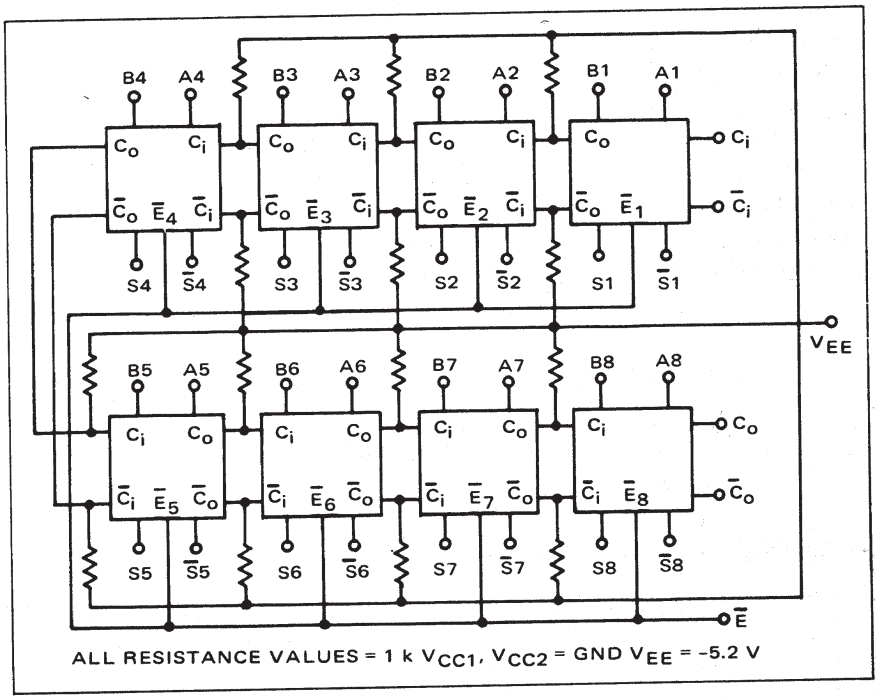


FIGURE 30 – 8-BIT FULL ADDER LOGIC DIAGRAM (MC1684F)

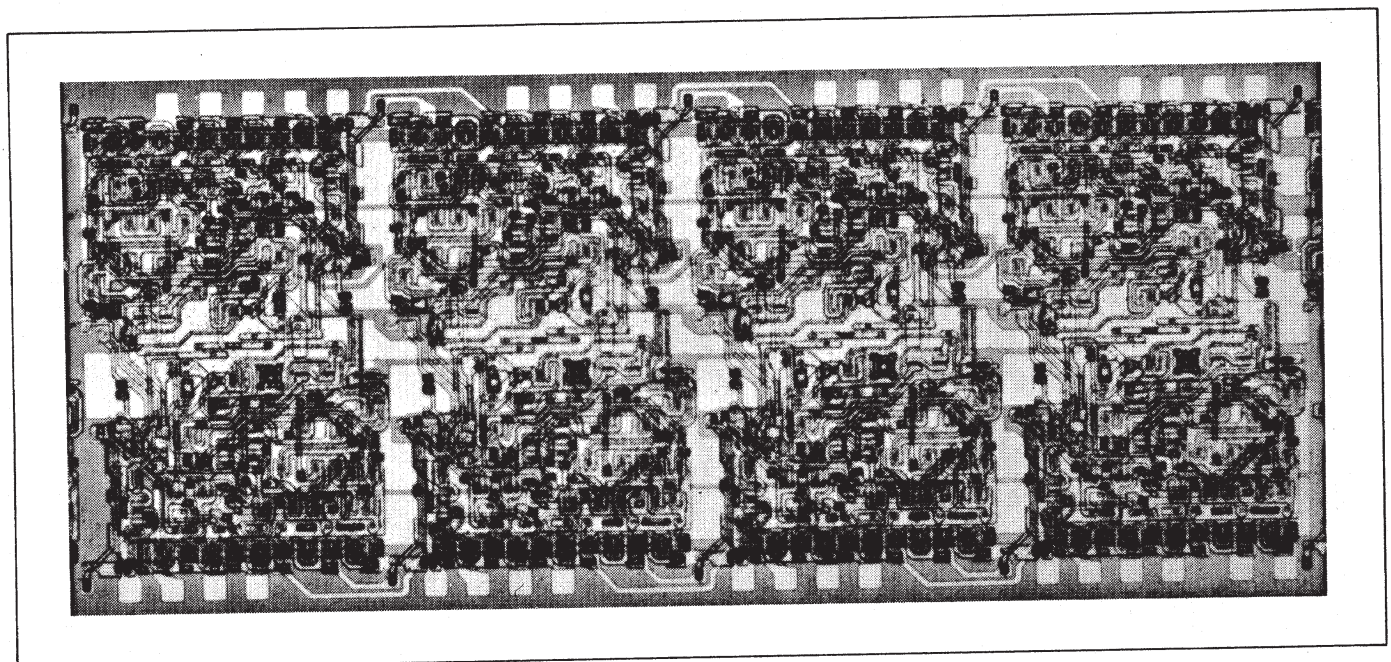


FIGURE 31 – GEOMETRY PHOTO OF 8-BIT FULL ADDER (MC1684F)

In addition to its extremely high operating speed, the 3-layers of metalization employed for the MECL III 8-bit full adder mark it as a unique product. The first layer of metalization intraconnects a majority of the components within each dual full adder assembly. The exceptions are a few critical crossovers that must be made in the second layer to eliminate problems of voltage distribution and routing interference. The second layer of metalization completes the dual full adders. The addition of the third layer of metalization interconnects all of the logic of the dual devices into one complete 8-bit full adder. This third layer also performs the overall power distribution function. A photomicrograph of the complete 8-bit full adder is shown in Figure 31.

Since the 8-bit full adder requires 37 pins for input and output functions the standard MECL III 15-pin stud mounted flat package obviously cannot be used. Instead, the 8-bit full adder die is mounted in a 40-pin ceramic flat pack. With adequate heat sinking, the packages can provide relatively constant junction temperature distribution between multiple 8-bit adder packages.

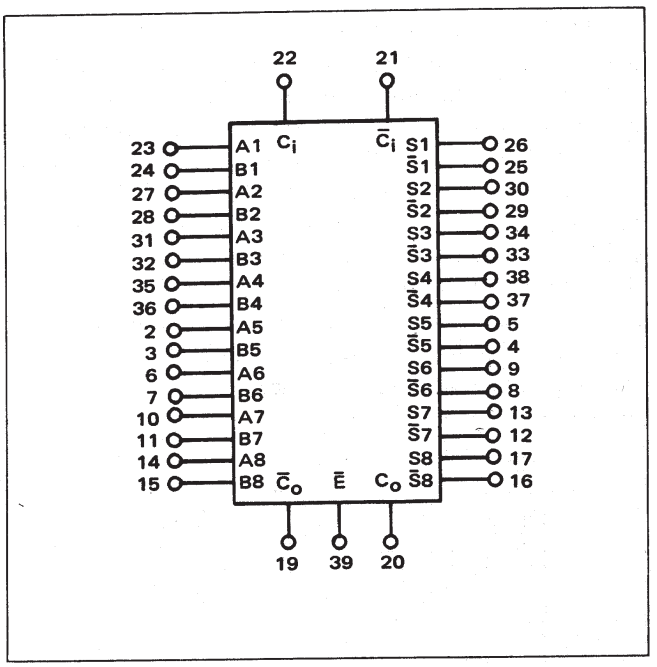


FIGURE 32 – 8-BIT FULL ADDER (MC1684F)

MECL III LINE SUMMARY
(PLANNED ADDITIONS ARE SHADED)

15 - PIN STUD-MOUNTED PACKAGE
V_{CC} (GND) PINS 1 AND 14, V_{EE} (-5.2 V ± 10%) STUD (PIN 15)
40 - PIN CERAMIC FLAT PACKAGE
V_{CC} (GND) PINS 1, AND 20; V_{EE} (-5.2 V ± 10%) PIN 40

GATES