MTTL

GENERAL INFORMATION SECTION

INTRODUCTION

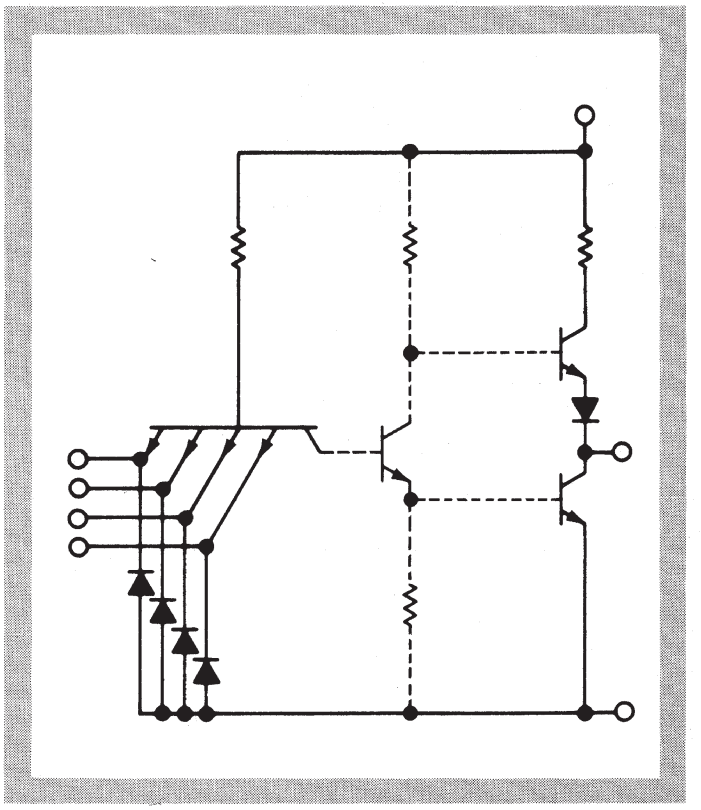
The MTTL MC7400P, MC5400L/7400L series of transistor-transistor logic is a medium-speed, high noise immunity family of saturating integrated logic circuits designed for general digital logic applications requiring clock frequencies to 30 MHz and switching speeds in the 12-15 ns range under moderate capacitive loading.

Though similar in circuitry to the MC500/400 series, the gates in this family have pin configurations compatible with the MDTL MC930/830 family of integrated circuits, with V_{CC} on pin 14 and ground on pin 7. (The MC500/400 series has V_{CC} on pin 4 and ground on pin 10.)

The circuits in the MC7400P, MC5400L/7400L series are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 – TYPICAL MTTL CIRCUIT
MC7400P, MC5400L/7400L Series



MAXIMUM RATINGS

Rating	Value	Unit
Supply Operating Voltage Range – MC5400 Series MC7400 Series	4.5 to 5.5 4.75 to 5.25	Vdc
Supply Voltage	+7.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range – MC5400 Series MC7400 Series	-55 to +125 0 to +70	°C
Storage Temperature Range – Ceramic Package Plastic Package	-65 to +150 -55 to +125	°C
Maximum Junction Temperature MC5400 Series MC7400 Series	 +175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Package Plastic Package	 0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Package Plastic Package	 0.26 0.30	°C/mW

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL MC7400P and MC5400L/7400L series. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range
- MC5400L Series = 4.5 to 5.5 volts
- MC7400P, L Series = 4.75 to 5.25 volts

Operating Temperature Range:
- MC5400L Series = −55 to +125°C
- MC7400P, L Series = 0 to +70°C

Output Drive Capability
- Other Gates (Output Loading Factor) = 10
- Capacitance = 600 pF

Output Impedance
- High State = 70 ohms (unsaturated) nominal
- Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
- +5.5 volts maximum
- −0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance
- High State = 400 k ohms nominal
- Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin
- High State — 0.400 volt minimum
- Low State — 0.400 volt minimum

Power Dissipation (1)
- Basic Gate = 10 mW typ/gate
- Basic Flip-Flop = 40 mW typ/pkg

Switching Speeds (2)
- Average Propagation Delay = 13 ns per gate typical
  30 ns per flip-flop typical
- Rise Time = 2.5 ns typical
- Fall Time = 1.5 ns typical

Flip-Flop Clock Frequency = 30 MHz maximum

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every eight packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL circuit.(1) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.30 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level, V_{OH} = 2.4 V minimum for the high-state output loading, with V_{IL} = 0.40 V, I_{OH} = −2.0 mA, and V_{CCL}.

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(1)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at V_{CC} = ±5.0 V.

(2) The switching characteristics of the MTTL family are defined with respect to the associated transistions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 6 (MC5450/7450) or 8 (MC5453/7453). Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

Three basic types of flip-flops are available in the MC7400P, MC5400L/7400L series: single and dual J-K, dual type D, and quad latch.

J-K Flip-Flop – MC7472P, MC5472L/7472L

This master-slave J-K flip-flop triggers on the negative edge of the clock. An AND-input configuration is used, consisting of three J inputs ANDed together and three K inputs ANDed together. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to permit presetting data into the flip-flop. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at the clocked inputs while the clock is in the low state since the master memory is inhibited in this condition. Information may be stored in the master flip-flop section when the clock goes high. Once the input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. They override the clock input and can be applied any time during the clock cycle.

The state of the master flip-flop is transferred to the slave flip-flop section on the negative transition of the clock, and the outputs respond accordingly. The flip-flop can be set or reset by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs. A special clamp circuit has been included on the clock line to guarantee that negative transients, such as ringing on the clock line, do not false-trigger the flip-flop. In addition, clamp diodes have been provided on all data inputs to limit any undershoot or negative ringing on the data lines.

Dual J-K Flip-Flop – MC7473P, MC5473L/7473L

This dual master-slave J-K flip-flop also triggers on the negative edge of the clock. Each of the independent flip-flops has a single J and a single K input. A direct $\overline{RESET}$ has been provided for preclearing the flip-flop regardless of the state of the clock. The operation of this device is the same as the MC7472P,MC5472L/7472L. Each of the flip-flops has the special clamp circuit on the clock line as well as clamp diodes on all the data inputs.

Dual J-K Flip-Flop – MC7476P

This dual master-slave J-K flip-flop is a 16-pin version of the MC7473P negative-edge-triggered flip-flop. It provides the direct $\overline{SET}$ input as well as the direct $\overline{RESET}$ input on each of the independent flip-flops. Operation is the same as for the MC7472P. This device is not available in the MC5400L/7400L series.

Dual Type D Flip-Flop – MC7479P, MC5479L/7479L

This positive-edge triggered Delay (type D) flip-flop provides a single clocked D input on each of the independent flip-flops. Direct $\overline{SET}$ and $\overline{RESET}$ inputs are available to precondition the state of the flip-flop. The flip-flop can be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the setup and hold times. The clocked inputs are inhibited when the clock is high; data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the setup and hold times is transferred to the bistable section on the positive edge of the clock, and the outputs respond accordingly. Clamp diodes have been provided on all data inputs to limit any possible undershoot on the data lines.

The characteristics of this flip-flop are better than those of many competitive types. The device is faster (f = 30 MHz typ, t_{pd} = 16 ns typ, compared to 25 MHz typ and 24 ns typ of competitive types). Propagation delays are symmetrical. Improved transfer characteristics are achieved by the use of an active pulldown. network. Input loading factors of 2 and 3 for the $\overline{SET}$ and $\overline{RESET}$ inputs respectively differ from competitive input load factors of 1 and 2 for the $\overline{SET}$ and $\overline{RESET}$ respectively.

Quad Latch – MC7475P

This quad latch consists of four gated single-input type D flip-flops. A common strobe line is provided for each pair of latches. Information is normally applied to the D input while the strobe is low since the flip-flop is inhibited in this condition. The type D flip-flop will respond to the data when the strobe goes high. The output will follow the data input as long as the strobe is in the high state. When the strobe goes low, the information that was present on the D input just before the transition of the strobe will be locked into the flip-flop. All of the inputs have clamp diodes to limit undershoot or negative ringing. This device is not available in the MC5400L/7400L series.

Noise Immunity

In a typical system noise begins to pose a problem when it is of such a magnitude that it can change the state of a flip-flop in the system or prevent a flip-flop from changing state at the proper time. Noise can be present on the ground line, the power supply line or the signal line.

In designing a system using MTTL, particular care must be taken due to the extremely high rate of change of voltage and current

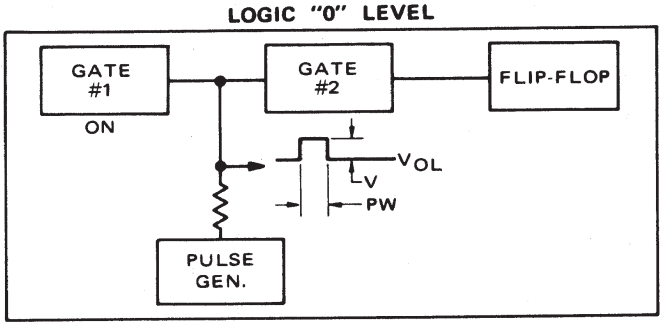
on the signal lines and current on the power supply and ground lines (see sections on Power and Ground Distribution and Bypassing). These factors increase the possibility of noise generation within the system itself in addition to externally generated noise.

Noise immunity in a digital system is a function of the propagation delays of the gates and flip-flops in the system and the dc threshold levels of these devices. The following block diagrams show typical test set-ups for measuring signal line, ground line and power supply line immunity of a gate in a digital system.

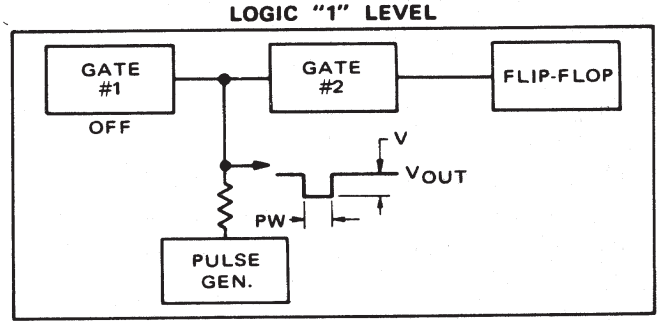
The system is considered disturbed when the flip-flop begins toggling. The curves show the typical noise amplitude a system can accept as a function of noise pulse width. As the pulse widths become narrower the amplitude can increase without disturbing the system. This can begin occurring when the pulse width is less than 20 ns on the signal line or 50 ns on the power supply or ground line. This pulse width-amplitude product is an indication of the minimum noise energy that is required to disturb a system. The low output impedance of MTTL gates and flip-flops requires more energy on the signal lines to disturb the system than in DTL or RTL systems. With proper power and ground distribution and bypassing, noise on power supply and ground lines can be maintained below levels which would be detrimental to system operation.

SIGNAL LINE NOISE IMMUNITY

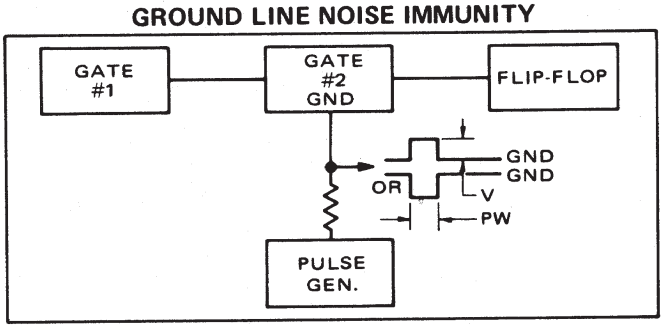
LOGIC "0" LEVEL



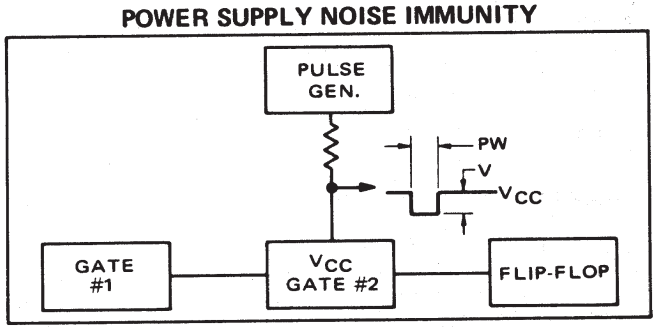
LOGIC "1" LEVEL



GROUND LINE NOISE IMMUNITY

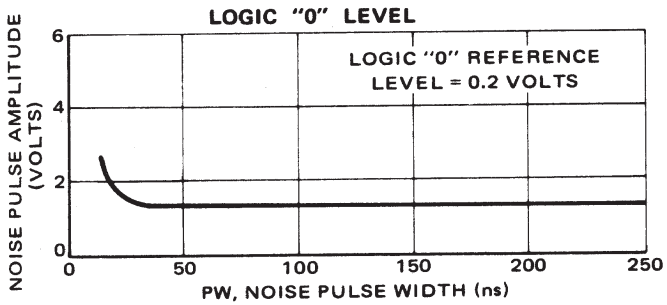


POWER SUPPLY NOISE IMMUNITY

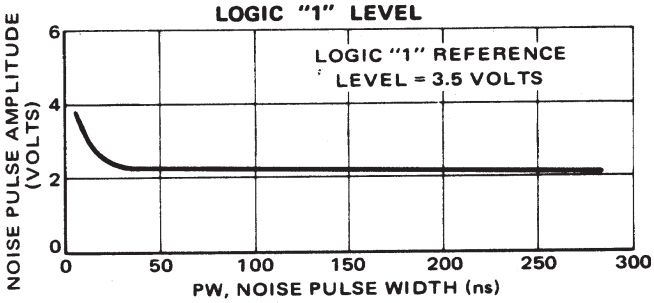


SIGNAL LINE NOISE IMMUNITY

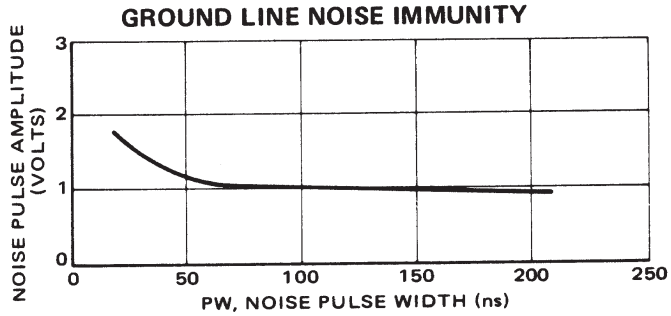
LOGIC "0" LEVEL



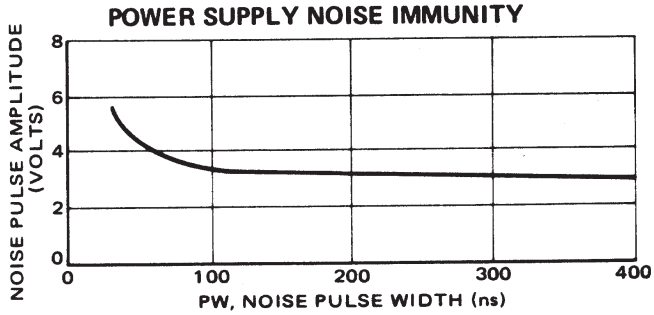
LOGIC "1" LEVEL



GROUND LINE NOISE IMMUNITY



POWER SUPPLY NOISE IMMUNITY



DEFINITIONS

C_T	Total parasitic capacitance, which include probe, wiring, and load capacitances	t_{pd+}	Turn-off delay time
f_{Tog}	Toggle frequency	t_{pd-}	Turn-on delay time
I_{CEX}	Collector-emitter leakage of the output transistor	t_{sd+}	Turn-off delay time from direct $\overline{SET}$ and $\overline{RESET}$ inputs
I_{DR}	Expander output drive current	t_{sd-}	Turn-on delay time from direct $\overline{SET}$ and $\overline{RESET}$ inputs
I_{EX}	Expander input current	TP_{in}	Test point at input of device under test
I_F	Input forward current	TP_{out}	Test point at output of device under test
I_{OH}	Output logic "1" state source current	V_{BE}	Base-emitter voltage
I_{OL}	Output logic "0" state sink current	V_{CC}	Power supply voltage
I_{PD}	Power supply current drain	V_{CCH}	Maximum operating power supply voltage
I_{PDH}	Power supply current drain with inputs in logic "1" state	V_{CCL}	Minimum operating power supply voltage
I_{PDL}	Power supply current drain with inputs in logic "0" state	V_{CEX}	Output transistor collector-emitter voltage
I_{R1}	Input reverse current with V_{IH} applied	V_{EN}	Input enable voltage level
I_{R2}	Input reverse current with V_{IHH} applied	V_{EX}	Expander terminal voltage
I_{SC}	Logic "1" state source current with output shorted to ground	V_{IH}	Logic "1" state input voltage
I_X	Expander terminal test current	V_{IHH}	Input breakdown voltage
PRF	Pulse repetition frequency	V_{IL}	Logic "0" state input voltage
R_{EX}	Resistor connected between expander terminals on expandable AOI gates	V_{INH}	Input inhibit voltage level
R_{EX1}	Resistor from expander output emitter to ground	V_{O1}	Expander output reverse voltage
R_{EX2}	Resistor from expander output collector to V_{CCL}	V_{O2}, V_{O3}	Expander output transistor emitter voltage
t+	Voltage rise time	V_{OH}	Logic "1" state output voltage
t-	Voltage fall time	V_{OL}	Logic "0" state output voltage
		V_R	Input reference voltage
		V_{th} "0"	Logic "0" state input threshold voltage
		V_{th} "1"	Logic "1" state input threshold voltage
		Z_{out}	Output impedance